



Silicon Gate MOS ROM 8316A

16,384 BIT STATIC MOS READ ONLY MEMORY

Organization—2048 Words x 8 Bits

Access Time—850 ns max

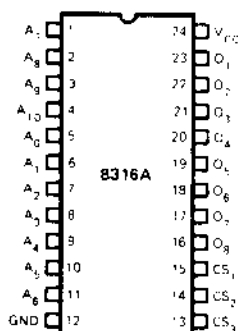
- Single +5 Volts Power Supply Voltage
- Directly TTL Compatible — All Inputs and Outputs
- Low Power Dissipation of 31.4 μ W/Bit Maximum
- Three Programmable Chip Select Inputs for Easy Memory Expansion
- Three-State Output — OR-Tie Capability
- Fully Decoded — On Chip Address Decode
- Inputs Protected — All Inputs Have Protection Against Static Charge

The Intel® 8316A is a 16,384-bit static MOS read only memory organized as 2048 words by 8 bits. This ROM is designed for microcomputer memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined and the desired chip select code is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitate easy memory expansion.

The 8316A read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible.

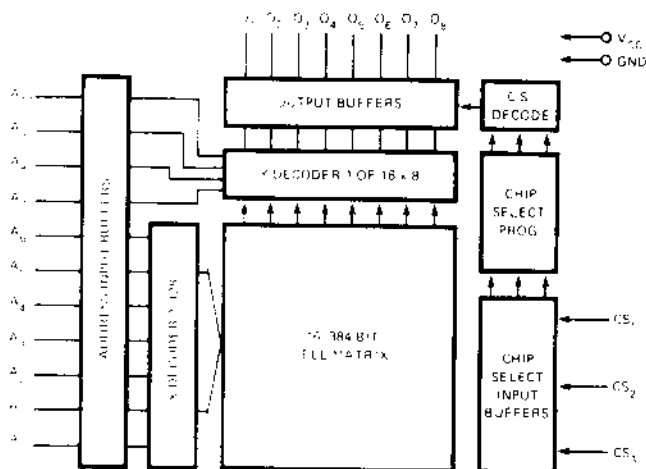
PIN CONFIGURATION



PIN NAMES

A_0 , A_{10}	ADDRESS INPUTS
O_1 , O_8	DATA OUTPUTS
CS_1 , CS_3	PROGRAMMABLE CHIP SELECT INPUTS

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect To Ground	-0.5V to +7V
Power Dissipation	1.0 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. ⁽¹⁾	MAX.		
I _{LI}	Input Load Current (All Input Pins)			10	μA	V _{IN} = 0 to 5.25V
I _{LOH}	Output Leakage Current			10	μA	CS = 2.2V, V _{OUT} = 4.0V
I _{LOL}	Output Leakage Current			-20	μA	CS = 2.2V, V _{OUT} = 0.45V
I _{CC}	Power Supply Current		40	98	mA	All inputs 5.25V Data Out Open
V _{IL}	Input "Low" Voltage	-0.5		0.8	V	
V _{IH}	Input "High" Voltage	2.0		V _{CC} +1.0V [†]	V	
V _{OL}	Output "Low" Voltage			0.45	V	I _{OL} = 2.0 mA
V _{OH}	Output "High" Voltage	2.2			V	I _{OH} = -100 μA

†1) Typical values for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP. ⁽¹⁾	MAX.	
t _{AD}	Address to Output Delay Time		400	850	nS
t _{CO}	Chip Select to Output Enable Delay Time			300	nS
t _{DF}	Chip Deselect to Output Data Float Delay Time	0		300	nS

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

Output Load . . . 1 TTL Gate, and C_{LOAD} = 100 pF
 Input Pulse Levels 0.8 to 2.0V
 Input Pulse Rise and Fall Times . (10% to 90%) 20 nS
 Timing Measurement Reference Level
 Input 1.5V
 Output 0.45V to 2.2V

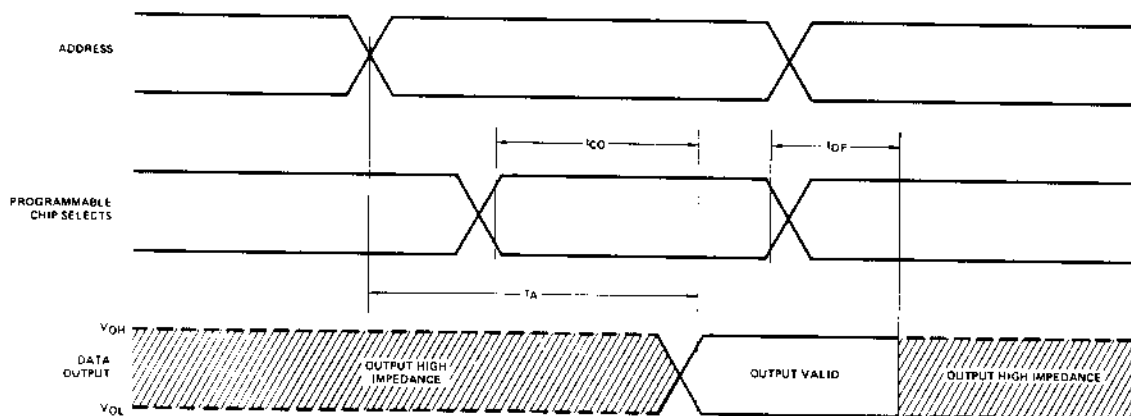
CAPACITANCE⁽²⁾ T_A = 25°C, f = 1 MHz

SYMBOL	TEST	LIMITS	
		TYP.	MAX.
C _{IN}	All Pins Except Pin Under Test Tied to AC Ground	4 pF	10 pF
C _{OUT}	All Pins Except Pin Under Test Tied to AC Ground	8 pF	15 pF

†2) This parameter is periodically sampled and is not 100% tested.

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WAVEFORMS

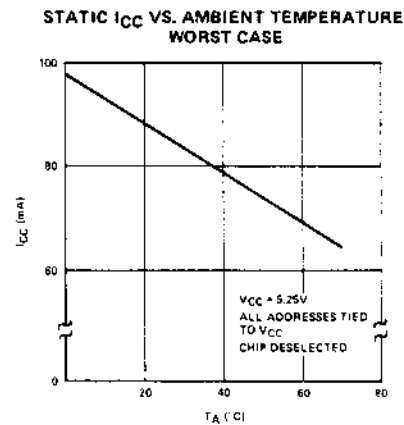
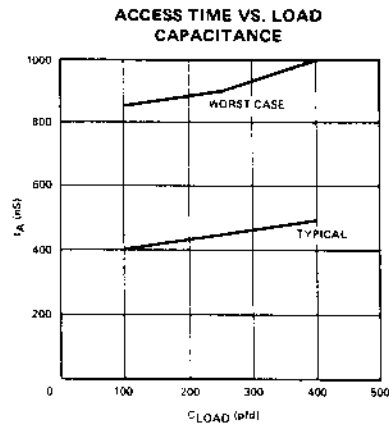
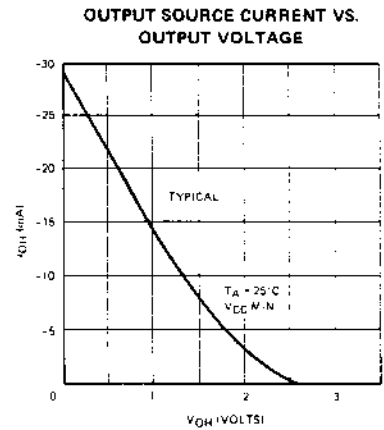
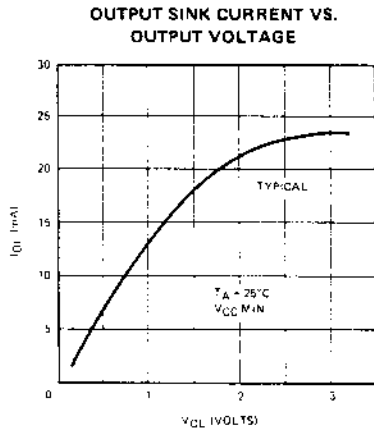
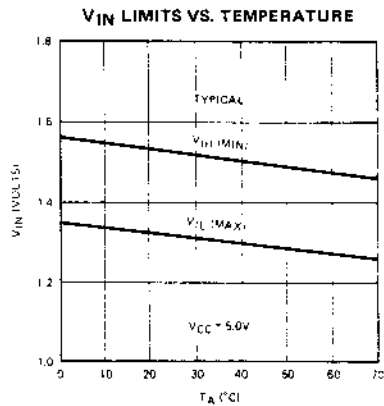
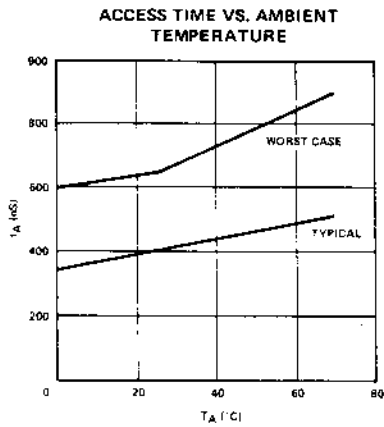


16K ROM PROTOTYPING

ROM systems may be developed and programs may be verified using Intel's 1702A or 2708 PROMs.

SILICON GATE MOS ROM 8316A

TYPICAL D.C. CHARACTERISTICS



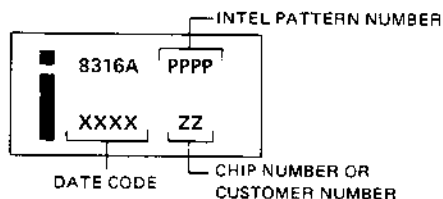
CUSTOMER _____	
P.O. NUMBER _____	
DATE _____	
For Intel use only	
S# _____	PPPP _____
STD _____	ZZ _____
_____	DD _____
APP _____	DATE _____

All custom 8316A ROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats designated on this order form. Additional forms are available from Intel.

MARKING

The marking as shown at the right must contain the Intel[®] logo, the product type (P8316A), the 4-digit Intel pattern number (PPPP), a date code (XXXX), and the 2-digit chip number (DD). An optional customer identification number may be substituted for the chip number (ZZ). Optional Customer Number (maximum 9 characters or spaces).

CUSTOMER NUMBER _____



MASK OPTION SPECIFICATIONS

A. CHIP NUMBER _____ (Must be specified—any number from 0 through 7-DD).

The chip number will be coded in terms of positive logic where a logic "1" is a high level input.

Chip Number	CS3	CS2	CS1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

B. ROM Truth Table Format

Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table should be accompanied with the order.

The following general format is applicable to the programming information sent to Intel:

- Data fields should be ordered beginning with the least significant address (0000) and ending with the most significant address (2047).
- A data field should start with the most significant bit and end with the least significant bit.

- The data field should consist of P's and N's. A P is to indicate a high level output (most positive) and an N a low level output (most negative). In terms of positive logic, a P is defined as a logic "1" and an N is defined as a logic "0". If the programming information is sent on a punched paper tape, then a start character, B, and an end character, F, must be used in the data field.

1. Punched Card Format

An 80-column Hollerith card (preferably interpreted) punched by an IBM 026 or 029 keypunch should be submitted. The first card will be a title card; the format is as follows:

MCS™ CUSTOM ROM ORDER FORM

a. Title Card

NO. OF OUTPUTS
4 or 8

TITLE CARD DESIGNATION

CUSTOMER'S COMPANY NAME

CUSTOMER'S DIVISION OR LOCATION

CUSTOMER'S PIN I

INTEL P.A. N

DECIMAL NUMBER INDICATING THE TRUTH TABLE NUMBER

Column	Data
1	Punch a T
2-5	Blank
6-30	Customer Company Name
31-34	Blank
35-54	Customer's Company Division or location
55-57	Blank
58-66	Customer Part Number
67	Blank
68-75	Punch the Intel 4-digit basic part number and in () the number of output bits, e.g., 8316A(8).
76-78	Blank
79-80	Punch a 2-digit decimal number to identify the truth table number (mask programmed chip select number).

b. For a 2048 word X 8-bit organization only, cards 2 and the following cards should be punched as shown.

MSB (OUTPUT 0)

LSB (OUTPUT 1)

8 DATA FIELDS

DECIMAL WORD ADDRESS BEGINNING EACH CARD

DECIMAL NUMBER INDICATING THE TRUTH TABLE NUMBER

Column	Data
1-5	Punch the 5-digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., 00000, 00008, 00016, etc.
6	Blank
7-14	Data Field
15	Blank
16-23	Data Field
24	Blank
25-32	Data Field
33	Blank
34-41	Data Field
42	Blank
43-50	Data Field
51	Blank
52-59	Data Field
60	Blank
61-68	Data Field
69	Blank
70-77	Data Field
78	Blank
79-80	Punch same 2-digit decimal number as in title card.

2. Paper Tape Format

1" wide paper tape using 7- or 8-bit ASCII code, such as a model 33 ASR teletype produces, or the 11/16" wide paper tape using a 5-bit Baudot code, such as a Telex produces.

The format requirements are as follows:

- All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly 2048 word fields for the 2048 X 8 ROM organization.
- Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F.

NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORD FIELD. If in preparing a tape an error is made, the entire word field, including the B and F, must be rubbed out. Within the word field, a P results in a high level output and an N results in a low level output.

c. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout or null punches (letter key for Telex tapes).

d. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted as a "comment"

just before each word field (or at least between every four word fields). When these carriage returns, etc., are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.

e. Included in the tape before the leader should be the customer's complete Telex or TWX number and, if more than one pattern is being transmitted, the ROM pattern number.

f. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

Start Character — Stop Character — Data Field — MSB — LSB

Leader: Rubout Key for TWX and Letter Key for Telex (at least 25 frames).

B P P P N N N N N F B N N N N N N P P F

Word Field 0 — Word Field 1 — Word Field 2048

Trailer: Rubout Key for TWX and Letter Key for Telex (at least 25 frames)